1. A method comprising:

providing a register accessible by a plurality of processors; and

indicating whether data in said register is available for a given processor.

2. The method of claim 1 including indicating for each of a plurality of processors whether the data is available for a given processor.

3. The method of claim 2 including requiring a processor to wait to execute an instruction until the data it needs to execute the instruction is available in one or more registers.

4. The method of claim 3 including providing a bit for each item of data indicating whether a given processor can access that data.

5. The method of claim 4 including resetting said bit when said data is accessed by a given processor.

6. The method of claim 5 including providing a register with a bit for each of a plurality processors, enabling a processor to reset said bit when the data is no longer useful to the processor, and preventing any processor from writing data to said register until all of

the bits indicate that the data is no longer useful to any other processor.

7. The method of claim 6 including indicating the processor which will utilize the data written into the register.

8. The method of claim 1 includes enabling a plurality of processors to access a register at the same time.

9. The method of claim 1 including providing specialized processors for mathematical operations and for memory.

10. The method of claim 1 including providing an input processor, an output processor and coupling said input, output and specialized processors to said register through a cross-bar connection.

11. An article comprising a medium storing instructions that enable a processor-based system to:

make a register accessible by a plurality of processing elements in said system; and

indicate whether data in said register is available for a given processing element.

12. The article of claim 11 further storing instructions that enable the processor-based system to determine whether data is available in a register for a particular processing element.

13. The article of claim 12 further storing instructions that enable the processor-based system to prevent execution of an instruction until the data needed to execute the instruction is available in one or more registers.

14. The article of claim 13 further storing instructions that enable the processor-based system to check a bit in said register for each item of data indicating whether a processing element can access said data.

15. The article of claim 14 further storing instructions that enable the processor-based system to reset said bit when said data is accessed by a processing element.

16. The article of claim 15 further storing instructions that enable the processor-based system to identify in said register a bit for a processing element from among bits for a plurality of processing elements, reset said bit when the data is no longer useful to a processing element, and to avoid writing said data to said

register until all the bits indicate that the data is no longer useful to any other processing element.

17. The article of claim 16 further storing instructions that enable the processor-based system to indicate which processing element will utilize the data written into the register by another processing element.

18. A digital signal processor including:

a plurality of processing elements; and

a register coupled to said plurality of processing elements, said register including a plurality of general purpose registers each accessible by said plurality of processing elements, at least one of said registers indicating whether data in said register is available for a given one of said plurality of processing elements.

19. The processor of claim 18 wherein said processing elements are coupled to said register by a cross-bar connection.

20. The processor of claim 18 including a plurality of registers each including a bit indicating for each of said processing elements whether the data in the general purpose register is available for a given processing element.

21. The processor of claim 18 wherein a processing element must wait to execute an instruction until the data it needs to execute the instruction is available in one or more general purpose registers.

22. The processor of claim 21 wherein each processing element has a designated bit for each general purpose register indicating whether a given processing element can access the data.

23. The processor of claim 18 wherein none of the processing elements can write data to a general purpose register until all of the bits indicate that the data is no longer useful to any other processing element.

24. The processor of claim 18 including a plurality of general purpose registers, each of said general purpose registers including a data section and a storage area for a bit for each of said plurality of processing elements.

25. The processor of claim 18 wherein said general purpose register is accessible by each of said processing elements at the same time.

26. The processor of claim 18 wherein at least one of said processing elements is an input processing element and another of said processing element an output processing element.

27. The processor of claim 26 further including at least one multiply and accumulate processing element.

28. The processor of claim 27 including at least one processing element for storing data in a random access memory.

29. The processor of claim 18 wherein no master processing element is included and instead, the sequence of operations in said digital signal processor is driven by the availability in a general purpose register of data needed to execute instructions.

30. The processor of claim 18 including a plurality of special purpose processing elements that may each access a register at the same time.